

CLAIMS

What is claimed is:

1 1. A phase offset cancellation circuitry comprising:
2 at least two phase detectors for receiving component clock signals of a multi-
3 phase clock generator, wherein at least some of the clock signals are offset from each other,
4 each of the at least two phase detectors for detecting phase differences between pairs of
5 component clock signals;
6 at least one summer coupled to the at least two phase detectors for measuring
7 the phase differences between the at least two phase detectors; and
8 at least one variable delay element for receiving the measured phase differences
9 and for providing a delay which is proportional to an output value of the at least one summer,
10 wherein the delay is used to reduce the phase difference between pairs of component clock
11 signals.

1 2. The system of claim 1 wherein each of the at least two phase detectors
2 measures a phase spacing of adjacent component clock signals.

1 3. The system of claim 1 wherein each of the at least two phase detectors
2 comprise:
3 a current source; and
4 two switches coupled to the current source, the two switches receiving a first
5 and a second component clock signal, wherein when the two switches are closed the phase

6 detector generates an indication of the difference between the first and second clock signals.

1 4. The system of claim 2 wherein the summer includes:
2 a mirror circuit coupled to the at least two phase detectors for detecting a
3 difference between the outputs of the at least two phase detectors; and
4 a capacitor coupled to the mirror circuit for charging or discharging based upon
5 the phase difference.

1 5. The system of claim 1 wherein the each of the at least two phase detectors
2 provides a voltage as an output.

1 6. The system of claim 1 wherein the each of the at least two phase detectors
2 provides a current as an output.

1 7. The system of claim 1 wherein each of the at least two phase detectors are
2 calibrated to minimize device mismatch within the phase detector.

1 8. A multi-phase clock generator comprising:
2 a plurality of clocks for clocking input data;
3 a plurality of samplers coupled to the plurality of docks for receiving the input
4 data, each of the samplers receiving a different clock phase; and
5 a phase offset cancellation system coupled to the plurality of clocks, the phase
6 offset cancellation system further comprising a plurality of phase detectors for receiving

7 component clock signals of the multi-phase clock generator, wherein at least some of the clock
8 signals are offset from each other, each of the plurality of phase detectors for detecting phase
9 differences between pairs of component clock signals; at least one summer coupled to the two
10 phase detectors for measuring the phase differences between the at least two phase detectors;
11 and at least one variable delay element for receiving the measured phase differences and for
12 providing a delay which is proportional to an output value of the at least one summer, wherein
13 the delay is used to reduce the phase difference between pairs of component clock signals.

1 9. The multi-phase clock generator of claim 8 wherein each of the at least two
2 phase detectors measures a phase spacing of adjacent clocks.

1 10. The multi-phase clock generator of claim 8 wherein each of the at least two
2 phase detectors comprise:
3 a current source; and
4 two switches coupled to the current source, the two switches receiving a first
5 and a second clock phase, wherein when the two switches are closed the phase detector
6 generates an indication of the difference between the first and second clock phases.

1 11. The multi-phase clock generator of claim 9 wherein the summer includes:
2 a mirror circuit coupled to the at least two phase detectors for detecting a
3 difference between the outputs of the at least two phase detectors; and
4 a capacitor coupled to the mirror circuit for charging or discharging based upon
5 the phase difference.

1 12. The multi-phase clock generator of claim 8 wherein the each of the at least two
2 phase detectors provides a voltage as an output.

1 13. The multi-phase clock generator of claim 8 wherein the each of the at least two
2 phase detectors provides a current as an output.

1 14. The multi-phase clock generator of claim 8 wherein each of the at least two
2 phase detectors are calibrated to minimize device mismatch within the phase detector.

1 15. A system for use with a multi-phase clock generator comprising:
2 a plurality of phase detectors coupled to the multiphase clock generator for
3 receiving clock phases from the multi-phase clock generator, wherein each of the phase
4 detectors measures a phase spacing of adjacent clocks; and
5 at least two phase detectors for receiving component clock signals of a multi-
6 phase clock generator, wherein at least some of the clock signals are offset from each other,
7 each of the phase detectors for detecting phase differences between pairs of component clock
8 signals;
9 at least one summer coupled to the at least two phase detectors for measuring
10 the phase differences between the at least two phase detectors; and
11 at least one variable delay element for receiving the measured phase differences
12 and for providing a delay which is proportional to an output value of the at least one summer,
13 wherein the delay is used to reduce the phase difference between pairs of component clock
14 signals.

1 16. The system of claim 15 wherein each of the plurality of phase detectors
2 comprises:
3 a current source; and
4 two switches coupled to the current source, the two switches receiving a first
5 and a second clock phase, wherein when the two switches are closed the phase detector
6 generates an indication of the difference between the first and second clock phases.

1 17. The system of claim 15 wherein each of the plurality of summers includes:
2 a mirror circuit coupled to at least two phase detectors for detecting a difference
3 between the outputs of the at least two phase detectors; and
4 a capacitor coupled to the mirror circuit for charging or discharging based upon
5 the phase difference.

1 18. The system of claim 17 wherein each of the at least two phase detectors are
2 calibrated to minimize device mismatch within the phase detector.

1 19. A circuit comprising:
2 a multi-phase clock generator; and
3 phase offset cancellation circuitry, coupled to the multi-phase clock generator,
4 the phase offset cancellation circuitry further comprising at least two phase detectors for
5 receiving component clock signals of a multi-phase clock generator, wherein at least some of
6 the clock signals are offset from each other, each of the phase detectors for detecting phase
7 differences between pairs of component clock signals; at least one summer coupled to the two

8 phase detectors for measuring the phase differences between the at least two phase detectors;
9 and at least one variable delay element for receiving the measured phase differences and for
10 providing a delay which is proportional to an output value of the at least one summer, wherein
11 the delay is used to reduce the phase difference between pairs of component clock signals.

1 20. A system comprising:
2 means for generating a multi-phase clock; and
3 means for cancelling phase offsets in the multi-phase clock, the phase offset
4 cancelling means comprising at least two phase detectors for receiving component clock
5 signals of a multi-phase clock generator, wherein at least some of the clock signals are offset
6 from each other, each of the phase detectors for detecting phase differences between pairs of
7 component clock signals; at least one summer coupled to the two phase detectors for
8 measuring the phase differences between the at least two phase detectors; and at least one
9 variable delay element for receiving the measured phase differences and for providing a delay
10 which is proportional to an output value of the at least one summer, wherein the delay is used
11 to reduce the phase difference between pairs of component clock signals.

1 21. A transmitter comprising:
2 a multi-phase clock generator;
3 phase offset cancellation circuitry for cancelling phase offsets of the multi-
4 phase clock generator, the phase offset cancellation circuitry being coupled to the multi-phase
5 clock generator, the phase offset cancellation circuitry further comprising at least two phase
6 detectors for receiving component clock signals of a multi-phase clock generator, wherein at

7 least some of the clock signals are offset from each other, each of the phase detectors for
8 detecting phase differences between pairs of component clock signals; at least one summer
9 coupled to the two phase detectors for measuring the phase differences between the at least two
10 phase detectors; and at least one variable delay element for receiving the measured phase
11 differences and for providing a delay which is proportional to an output value of the at least
12 one summer, wherein the delay is used to reduce the phase difference between pairs of
13 component clock signals; and
14 a driver that is clocked by the phase offset cancelled multi-phase clock
15 generator.

1 22. A receiver comprising:
2 a multi-phase clock generator;
3 phase offset cancellation circuitry for cancelling phase offsets of the multi-
4 phase clock generator, the phase offset cancellation circuitry being coupled to the multi-phase
5 clock generator, the phase offset cancellation circuitry further comprising at least two phase
6 detectors for receiving component clock signals of a multi-phase clock generator, wherein at
7 least some of the clock signals are offset from each other, each of the phase detectors for
8 detecting phase differences between pairs of component clock signals; at least one summer
9 coupled to the two phase detectors for measuring the phase differences between the at least two
10 phase detectors; and at least one variable delay element for receiving the measured phase
11 differences and for providing a delay which is proportional to an output value of the at least
12 one summer, wherein the delay is used to reduce the phase difference between pairs of
13 component clock signals; and

14 a sampler that is clocked by the phase offset cancelled multi-phase clock
15 generator.

1 23. A system comprising:
2 a multi-phase clock generator;
3 a receiver coupled to the multi-phase clock generator;
4 a transmitter coupled to the multi-phase clock generator; and
5 phase offset cancellation circuitry for cancelling phase offsets of the multi-
6 phase clock generator, the phase offset cancellation circuitry being coupled to the multi-phase
7 clock generator, the phase offset cancellation circuitry further comprising at least two phase
8 detectors for receiving component clock signals of a multi-phase clock generator, wherein at
9 least some of the clock signals are offset from each other, each of the phase detectors for
10 detecting phase differences between pairs of component clock signals; at least one summer
11 coupled to the two phase detectors for measuring the phase differences between the at least two
12 phase detectors; and at least one variable delay element for receiving the measured phase
13 differences and for providing a delay which is proportional to an output value of the at least
14 one summer, wherein the delay is used to reduce the phase difference between pairs of
15 component clock signals, wherein the transmitter and/or receiver utilize the phase offset
16 cancelled multiphase clock generator.